

FEATURES

- Provides six ultra-low skew copies of the selected input
- 2:1 MUX input included for clock switchover applications
- Guaranteed AC performance over temperature and voltage:
 - Clock frequency range: DC to > 6GHz
 - <300ps IN-to-OUT t_{pd}
 - <80ps t_r / t_f times
 - <20ps skew (output-to-output)
- Ultra-low jitter design:
 - <1ps_{RMS} random jitter
 - <10ps_{pp} total jitter (clock)
 - <1ps_{RMS} cycle-to-cycle jitter
 - <0.7ps_{RMS} crosstalk-induced jitter
- Low supply voltage operation: 2.5V and 3.3V
- Unique input termination and VT pin accepts DC-coupled and AC-coupled inputs (CML, PECL, LVDS)
- Unique input isolation design minimizes crosstalk
- 400mV LVPECL (100K compatible) output swing
- -40°C to +85°C temperature range
- Available in 32-pin (5mm x 5mm) MLF® package



Precision Edge®

DESCRIPTION

The SY58036U is a 2.5V/3.3V precision, high-speed, 1:6 fanout buffer capable of handling clocks up to 6GHz. A differential 2:1 MUX input is included for redundant clock switchover applications.

The differential input includes Micrel's unique, 3-pin input termination architecture that allows the device to interface to any differential signal (AC- or DC-coupled) as small as 100mV without any level shifting or termination resistor networks in the signal path. The outputs are 400mV LVPECL (100K temperature compensated), with extremely fast rise/fall times guaranteed to be less than 80ps.

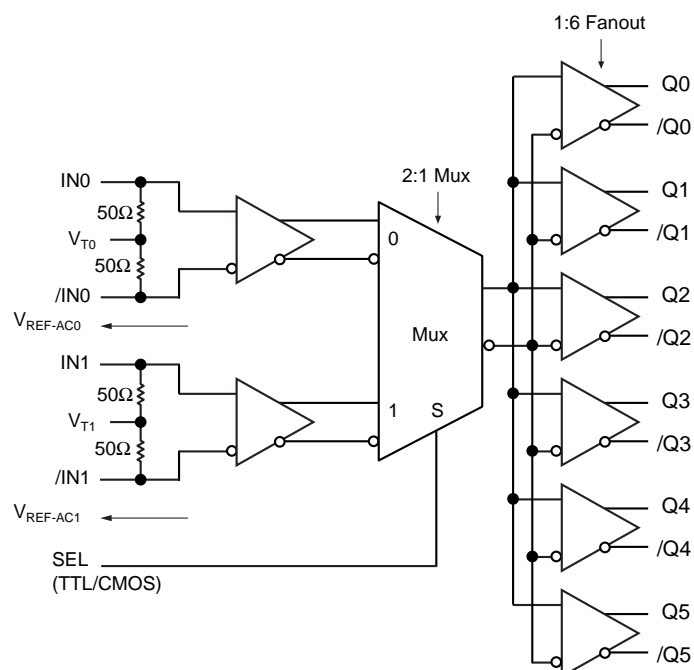
The SY58036U operates from a 2.5V ±5% supply or a 3.3V ±10% supply and is guaranteed over the full industrial temperature range of -40°C to +85°C. For applications that require CML outputs, consider the SY58034U or for 800mV LVPECL outputs the SY58035U. The SY58036U is part of Micrel's high-speed, Precision Edge® product line.

All support documentation can be found on Micrel's web site at www.micrel.com.

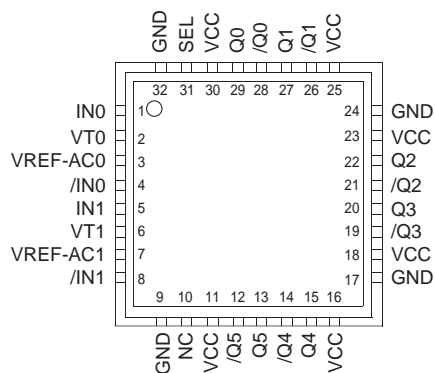
APPLICATIONS

- Redundant clock distribution
- All SONET/SDH clock distribution
- All Fibre Channel distribution
- All Gigabit Ethernet clock distribution

FUNCTIONAL BLOCK DIAGRAM



PACKAGE/ORDERING INFORMATION



32-Pin MLF® (MLF-32)

Ordering Information⁽¹⁾

| Part Number | Package Type | Operating Range | Package Marking | Lead Finish |
|--------------------------------|--------------|-----------------|--|----------------|
| SY58036UMI | MLF-32 | Industrial | SY58036U | Sn-Pb |
| SY58036UMITR ⁽²⁾ | MLF-32 | Industrial | SY58036U | Sn-Pb |
| SY58036UMG(3) | MLF-32 | Industrial | SY58036U with Pb-Free bar-line indicator | NiPdAu Pb-Free |
| SY58036UMGTR ^(2, 3) | MLF-32 | Industrial | SY58036U with Pb-Free bar-line indicator | NiPdAu Pb-Free |

Notes:

1. Contact factory for die availability. Dice are guaranteed at T_A = 25°C, DC electricals only.
2. Tape and Reel.
3. Pb-Free package recommended for new designs.

PIN DESCRIPTION

| Pin Number | Pin Name | Pin Function |
|--|---|--|
| 1, 4 5, 8 | IN0, /IN0 IN1, /IN1 | Differential Input: These input pairs are the differential signal inputs to the device. These inputs accept AC- or DC-coupled signals as small as 100mV. Each pin of a pair internally terminates to a VT pin through 50Ω. Note that these inputs will default to an indeterminate state if left open. Please refer to the "Input Interface Applications" section for more details. |
| 2, 6 | VT0, VT1 | Input Termination Center-Tap: Each side of the differential input pair terminates to a VT pin. The VT0 and VT1 pins provide a center-tap to a termination network for maximum interface flexibility. See "Input Interface Applications" section for more details. |
| 31 | SEL | This single-ended TTL/CMOS compatible input selects the inputs to the multiplexer. Note that this input is internally connected to a 25kΩ pull-up resistor and will default to a logic HIGH state if left open. The MUX select switchover function is asynchronous. |
| 10 | NC | No connect. |
| 11, 16, 18, 23, 25, 30 | VCC | Positive Power Supply: Bypass with 0.1μF ^T ™0.01μF low ESR capacitors and place as close to the VCC pins as possible. |
| 29, 28 27, 26 22, 21 20, 19 15, 14 13, 12 | Q0, /Q0, Q1, /Q1, Q2, /Q2, Q3, /Q3, Q4, /Q4, Q5, /Q5 | Differential Outputs: These 100K (temperature compensated) LVPECL output pairs are low skew copies of the selected input. Please refer to the "Truth Table" for details. |
| 9, 17, 24, 32 | GND, Exposed Pad | Ground. Ground pin and exposed pad must be connected to the same ground plane. |
| 3, 7 | VREF-AC0 VREF-AC1 | Reference Voltage: These output biases to V _{CC} -1.2V. It is used for AC-coupling inputs (IN, /IN). Connect V _{REF-AC} directly to the VT pin. Bypass with 0.01μF low ESR capacitor to V _{CC} . See "Input Interface Applications" section. Maximum sink/source current is ±1.5mA. Due to the limited drive capability, the VREF-AC pin is only intended to drive its respective VT pin. |

TRUTH TABLE

| SEL | |
|-----|--------------------|
| 0 | IN0 Input Selected |
| 1 | IN1 Input Selected |

Absolute Maximum Ratings⁽¹⁾

| | |
|---------------------------------------|-------------------|
| Power Supply Voltage (V_{CC}) | -0.5V to +4.0V |
| Input Voltage (V_{IN}) | -0.5V to V_{CC} |
| LVPECL Output Current (I_{OUT}) | |
| Continuous | 50mA |
| Surge | 100mA |
| Termination Current | |
| Source or sink current on V_T pin | ±100mA |
| Input Current | |
| Source or sink current on IN, /IN pin | ±50mA |
| Source or sink current on VREF-AC pin | ±2mA |
| Lead Temperature (soldering, 10 sec.) | 220°C |
| Storage Temperature Range (T_S) | -65°C to +150°C |

Operating Ratings⁽²⁾

| | |
|---|--------------------|
| Power Supply Voltage (V_{CC}) | +2.375V to +2.625V |
| | +3.0V to +3.6V |
| Ambient Temperature Range (T_A) | -40°C to +85°C |
| Package Thermal Resistance ⁽³⁾ | |
| MLF® (θ_{JA}) | |
| Still-Air | 35°C/W |
| MLF® (ψ_{JB}) | |
| Junction-to-Board | 16°C/W |

DC ELECTRICAL CHARACTERISTICS⁽⁴⁾

$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, unless otherwise stated.

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|----------------|---|------------------------|--------------|--------------|--------------|-------|
| V_{CC} | Power Supply Voltage | | 2.375 | 2.5 | 2.625 | V |
| | | | 3.0 | 3.3 | 3.6 | V |
| I_{CC} | Power Supply Current | No load, max. V_{CC} | | 180 | 250 | mA |
| R_{DIFF_IN} | Differential Input Resistance (IN-to-/IN) | | 90 | 100 | 110 | Ω |
| R_{IN} | Input Resistance (IN-to- V_T) | | 45 | 50 | 55 | Ω |
| V_{IH} | Input HIGH Voltage (IN, /IN) | Note 5 | $V_{CC}-1.6$ | | V_{CC} | V |
| V_{IL} | Input LOW Voltage (IN, /IN) | | 0 | | $V_{IH}-0.1$ | V |
| V_{IN} | Input Voltage Swing (IN, /IN) | See Figure 1a. | 0.1 | | 1.7 | V |
| V_{DIFF_IN} | Differential Input Voltage Swing IN, /IN | See Figure 1b. | 0.2 | | | V |
| V_{T_IN} | IN to V_T (IN, /IN) | | | | 1.28 | V |
| V_{REF-AC} | Reference Voltage | | $V_{CC}-1.3$ | $V_{CC}-1.2$ | $V_{CC}-1.1$ | V |

Notes:

1. Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.
2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.
3. Thermal performance assumes exposed pad is soldered (or equivalent) to the device's most negative potential on the PCB. ψ_{JB} and θ_{JA} are shown for a 4-layer PCB in a still air environment, unless otherwise stated.
4. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.
5. V_{IH} (min) not lower than 1.2V.

LVPECL OUTPUT DC ELECTRICAL CHARACTERISTICS⁽⁶⁾

$V_{CC} = 2.5V \pm 5\%$ or $3.3V \pm 10\%$, $R_L = 50\Omega$ to $V_{CC}-2V$; $T_A = -40^\circ C$ to $+85^\circ C$, unless otherwise stated.

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|-----------------|-----------------------------------|----------------|----------------|-----|----------------|-------|
| V_{OH} | Output HIGH Voltage | | $V_{CC}-1.145$ | | $V_{CC}-0.895$ | V |
| V_{OL} | Output LOW Voltage | | $V_{CC}-1.545$ | | $V_{CC}-1.295$ | V |
| V_{OUT} | Output Differential Swing | See Figure 1a. | 150 | 400 | | mV |
| V_{DIFF_OUT} | Differential Output Voltage Swing | See Figure 1b. | 300 | 800 | | mV |

LVTTTL/CMOS DC ELECTRICAL CHARACTERISTICS⁽⁶⁾

$V_{CC} = 2.5V \pm 5\%$ or $3.3V \pm 10\%$; $T_A = -40^\circ C$ to $+85^\circ C$, unless otherwise stated.

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|----------|--------------------|-----------|------|-----|-----|---------|
| V_{IH} | Input HIGH Voltage | | 2.0 | | | V |
| V_{IL} | Input LOW Voltage | | | | 0.8 | V |
| I_{IH} | Input HIGH Current | | -125 | | 40 | μA |
| I_{IL} | Input LOW Current | | -300 | | | μA |

Note:

6. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

AC ELECTRICAL CHARACTERISTICS⁽⁷⁾

$V_{CC} = 2.5V \pm 5\%$ or $3.3V \pm 10\%$, $R_L = 50\Omega$ to $V_{CC}-2V$; $T_A = -40^\circ C$ to $+85^\circ C$, unless otherwise stated.

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|------------------------|---|------------------------|----------------|-----|-----|-------------------|
| f_{MAX} | Maximum Operating Frequency | $V_{OUT} \geq 200mV$ | 6 | 7 | | GHz |
| t_{pd} | Differential Propagation Delay (IN0 or IN1-to-Q) (SEL-to-Q) | | 150 | 220 | 300 | ps |
| | | | 100 | 220 | 400 | ps |
| Δt_{pd} Tempco | Differential Propagation Delay Temperature Coefficient | | | 65 | | fs/°C |
| t_{SKEW} | Output-to-Output | Note 8 | | | 20 | ps |
| | Part-to-Part | Note 9 | | | 100 | ps |
| t_{JITTER} | Clock | Cycle-to-Cycle Jitter | Note 10 | | 1 | ps _{RMS} |
| | | Random Jitter (RJ) | Note 11 | | 1 | ps _{RMS} |
| | | Total Jitter (TJ) | Note 12 | | 10 | ps _{PP} |
| | Adjacent Channel Crosstalk-Induced Jitter | Note 13 | | | 0.7 | ps _{RMS} |
| t_r, t_f | Output Rise/Fall Time | Full Swing, 20% to 80% | 20 | 40 | 80 | ps |

Notes:

- 7. High frequency AC electricals are guaranteed by design and characterization.
- 8. Output-to-output skew is measured between outputs under identical transitions.
- 9. Part-to-part skew is defined for two parts with identical power supply voltages at the same temperature and with no skew of the edges at the respective inputs.
- 10. Cycle-to-cycle jitter definition: the variation of periods between adjacent cycles, $T_n - T_{n-1}$ where T is the time between rising edges of the output signal.
- 11. Random jitter is measured with a K28.7, measured at 2.5Gbps.
- 12. Total jitter definition: with an ideal clock input of frequency - f_{MAX} , no more than one output edge in 10^{12} output edges will deviate by more than the specified peak-to-peak jitter value.
- 13. Crosstalk is measured at the output while applying two similar clock frequencies that are asynchronous with respect to each other at the inputs.

SINGLE-ENDED AND DIFFERENTIAL SWINGS

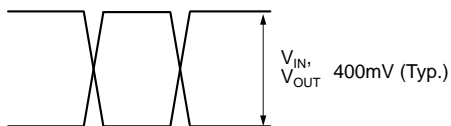


Figure 1a. Single-Ended Voltage Swing

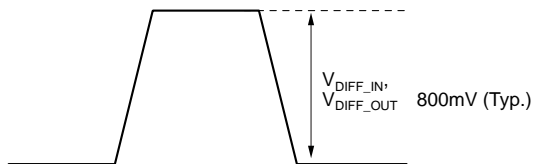
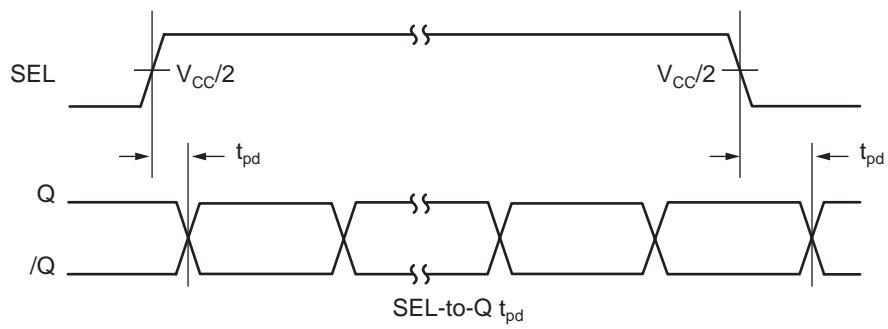
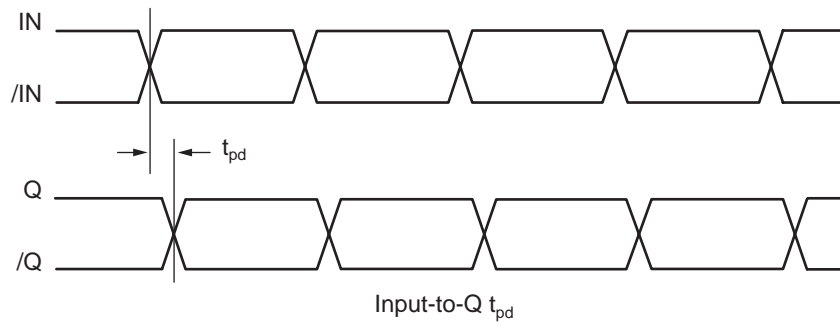


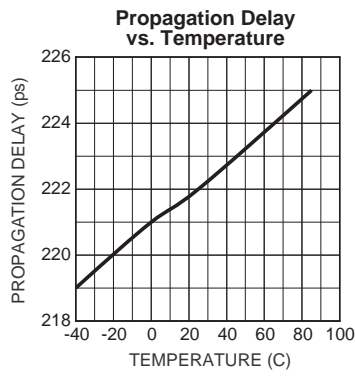
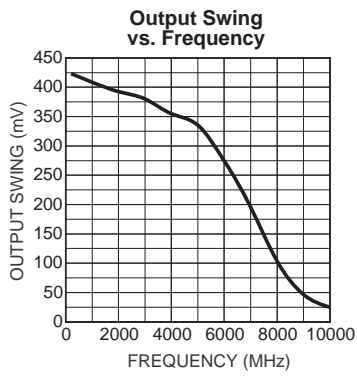
Figure 1b. Differential Voltage Swing

TIMING DIAGRAMS



TYPICAL OPERATING CHARACTERISTICS

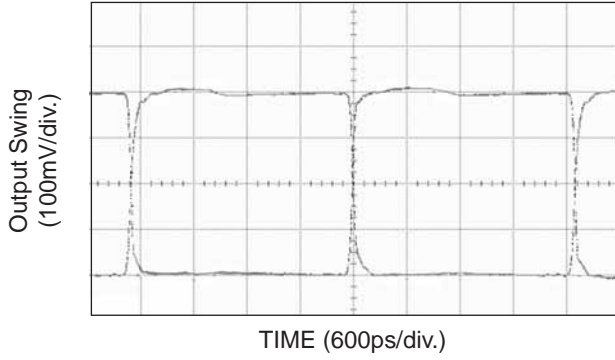
$V_{CC} = 2.5V$, $GND = 0$, $V_{IN} = 100mV$, $R_L = 50\Omega$ to $V_{CC}-2V$; $T_A = 25^\circ C$, unless otherwise stated.



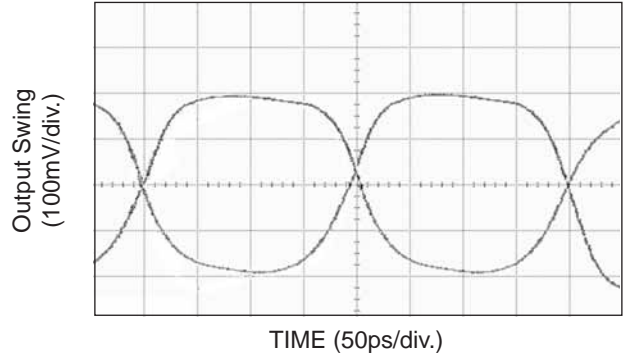
FUNCTIONAL CHARACTERISTICS

$V_{CC} = 3.3V$, $GND = 0$, $V_{IN} = 100mV$, $R_L = 50\Omega$ to $V_{CC}-2V$; $T_A = 25^\circ C$, unless otherwise stated.

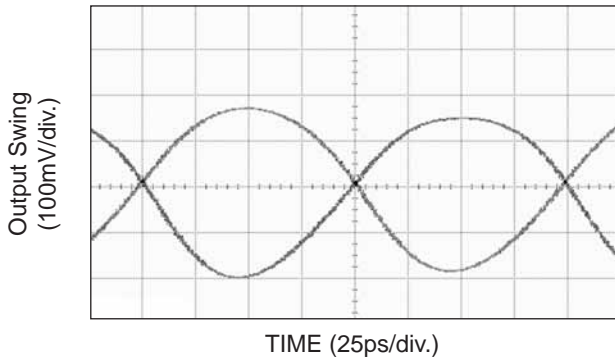
200MHz Output



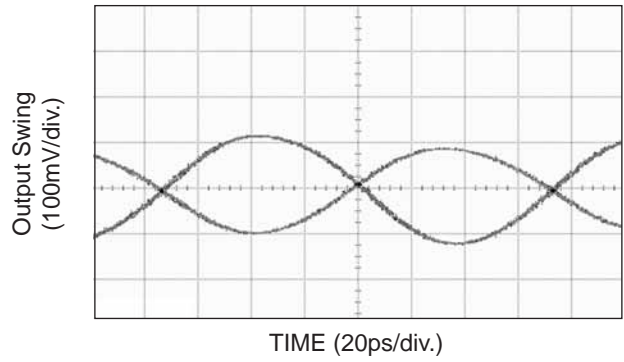
2.5GHz Output



5GHz Output



7GHz Output



INPUT AND OUTPUT STAGES

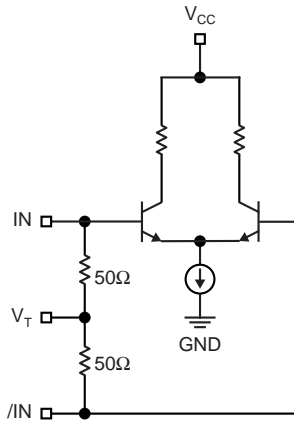


Figure 2a. Simplified Differential Input Stage

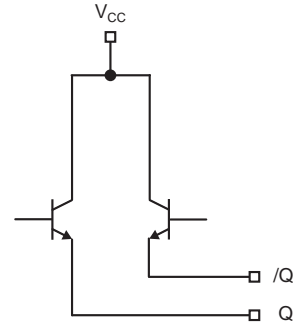


Figure 2b. Simplified LVPECL Output Stage

INPUT INTERFACE APPLICATIONS

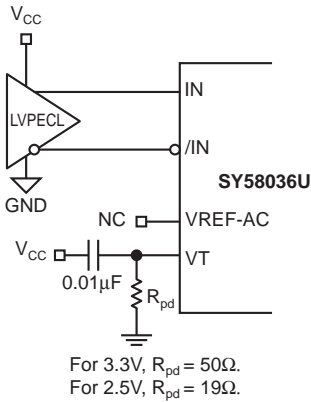


Figure 3a. LVPECL Interface (DC-Coupled)

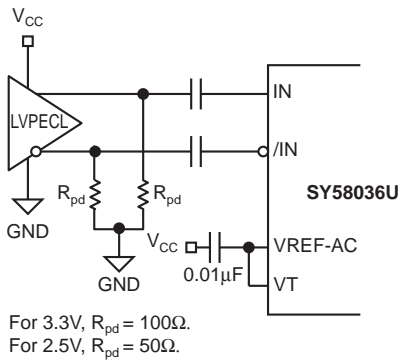


Figure 3b. LVPECL Interface (AC-Coupled)

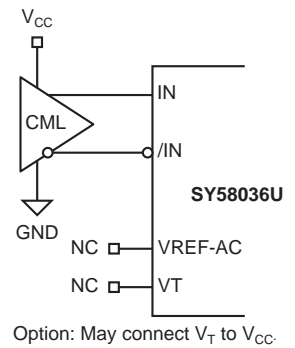


Figure 3c. CML Interface (DC-Coupled)

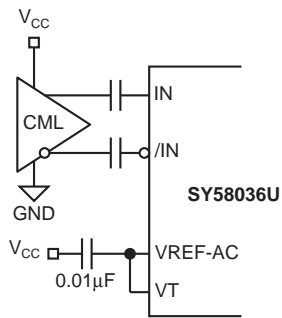


Figure 3d. CML Interface (AC-Coupled)

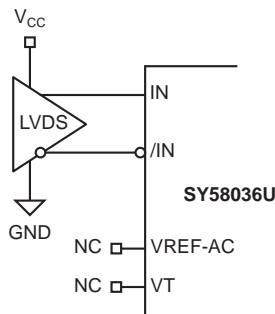


Figure 3e. LVDS Interface

OUTPUT INTERFACE APPLICATIONS

LVPECL has high input impedance, very low output (open emitter) impedance, and small signal swing, which results in low EMI. LVPECL is ideal driving 50Ω and 100Ω controlled impedance transmission lines. There are several techniques

for terminating the LVECL output: parallel-thevenin equivalent termination and parallel termination (3-resistor). Unused output pairs may be left floating. However, single-ended outputs must be terminated, or balanced.

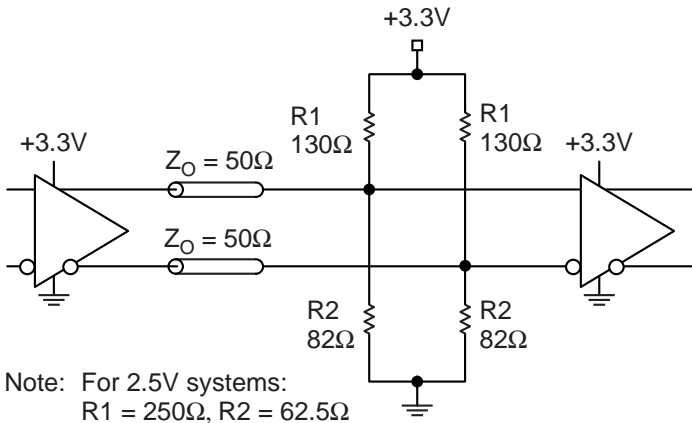


Figure 4a. Parallel Thevenin-Equivalent Termination

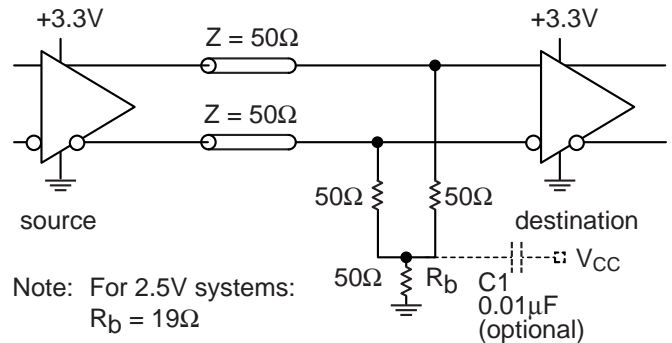
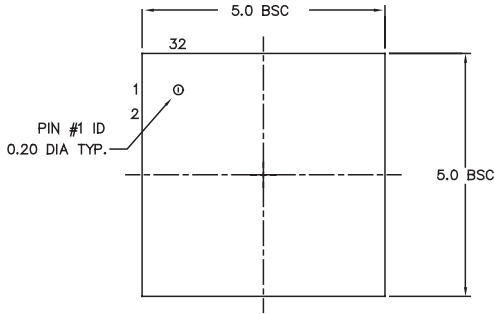


Figure 4b. Parallel Termination (3-Resistor)

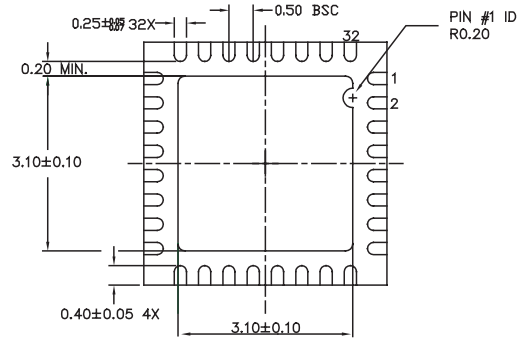
RELATED MICREL PRODUCTS AND SUPPORT DOCUMENTATION

| Part Number | Function | Data Sheet Link |
|---------------|--|--|
| SY58034U | 6GHz, 1:6 CML Fanout Buffer with 2:1 MUX Input and Internal I/O Termination | http://www.micrel.com/product-info/products/sy58034u.shtml |
| SY58035U | 4.5GHz, 1:6 LVPECL Fanout Buffer with 2:1 MUX Input and Internal Termination | http://www.micrel.com/product-info/products/sy58035u.shtml |
| | MLF® Application Note | www.amkor.com/products/notes_papers/MLF_AppNote_0902.pdf |
| HBW Solutions | New Products and Applications | www.micrel.com/product-info/products/solutions.shtml |

32-PIN MicroLeadFrame® (MLF-32)



TOP VIEW

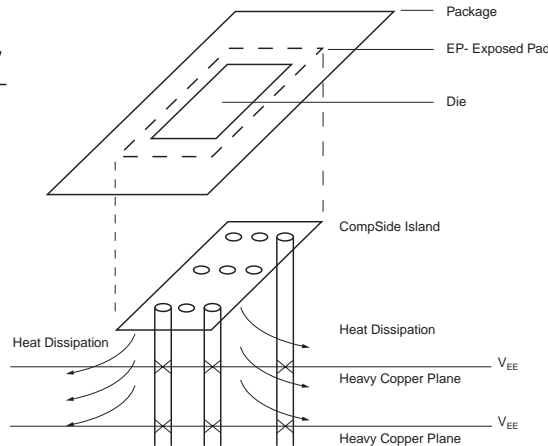


BOTTOM VIEW



SIDE VIEW

- NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
 2. MAX. PACKAGE WARPAGE IS 0.05 mm.
 3. MAXIMUM ALLOWABLE BURRS IS 0.076 mm IN ALL DIRECTIONS.
 4. PIN #1 ID ON TOP WILL BE LASER/INK MARKED.



**PCB Thermal Consideration for 32-Pin MLF® Package
(Always solder, or equivalent, the exposed pad to the PCB)**

Package Notes:

1. Package meets Level 2 qualification.
2. All parts are dry-packaged before shipment.
3. Exposed pads must be soldered to a ground for proper thermal management.

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